REMARKS

Reconsideration and allowance of the above-identified application are respectfully requested.

Claims 2-4, 7, 8, 11, 12, 14-16, 19, 20, 23-25 and 27-33 are currently pending, wherein claims 2, 3, 14, 15, 23, 24, 29 and 30 are independent. Claims 1, 5, 6, 9, 10, 13, 17, 18, 21, 22 and 26 have been canceled. Claims 2-4, 7, 8, 11, 12, 14-16, 19, 20, 23-25, 27-30 have been amended. Claims 31-33 have been added.

Claims 2, 3, 14, 15, 23 and 24 have been amended merely to write these claims in independent form, including all of the limitations of the base claim and any intervening claims. Dependent claims 4, 7, 8, 11, 12, 16, 19, 20, 25, 27 and 28 have been amended merely to change the dependency of these claims. These amendments do not narrow or otherwise limit the claims, are not made for any purpose related to patentability, and are fully supported by present application. Claims 29 and 30 have been amended to recite that the heat sink can be substantially thermally isolated from the planar package substrate. Support for these amendments can be found in, for example, original claims 3, 15 and 24. Support for new claims 31 and 33 can be found at least on Page 6, Paragraph 0017 of the present application, while support for new claim 32 can be found at least on Page 8, Paragraph 0018. No new matter has been introduced by way of these amendments or new claims.

Applicant notes with appreciation the acknowledgment of the Information Disclosure Statement previously submitted to the Patent Office on January 14, 2004.

Applicant would like to thank Examiner Alexander Williams for the interview conducted on July 7, 2004. In compliance with M.P.E.P. § 713.04, the substance of that interview is incorporated in the foregoing amendments and following remarks.

In the first section of the Office Action, the disclosure is objected, because the divisional application information should be updated. This objection is respectfully traversed.

Although several divisional applications have been filed claiming priority to the present (parent) application, Applicant respectfully notes that the present application is the original, parent application filed in this "family" of applications. Therefore, Applicant respectfully submits that there is no divisional application information for the present application with which to update the disclosure of the present application. Accordingly, reconsideration and withdrawal of these grounds of objection are respectfully requested.

During the interview, claims 2 and 3 were discussed. In particular, the rejection of claims 2-4, 7, 8, 11, 12, 14-16, 19, 20, 23-25 and 27-30 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Shiraishi et al. (U.S. Patent No. 6,525,414, hereinafter "Shiraishi") in view of Kato et al. (U.S. Patent No. 5,424,573, hereinafter "Kato") was discussed. No agreement was reached. This rejection is respectfully traversed.

Exemplary embodiments of the present invention are directed to an integrated chip package that provides a low cost package that is suitable for high-density semiconductors that have high power dissipation. The integrated chip package includes at least one semiconductor chip having a first surface and a second surface. The first surface of the semiconductor chip is electrically coupled to an intermediate substrate via conductive bumps. The intermediate substrate is also electrically coupled to a package substrate via a plurality of bonding wires. The second surface of the semiconductor chip is thermally coupled to a heat sink to increase the power dissipation capacity of the integrated chip package. Consequently, the thermal path of the integrated chip package extends to the heat sink away from the

package substrate, thereby reducing the heat load of the circuit board or circuit substrate to which the integrate chip package is connected. [*see* present application, page 5, paragraph 0016]

Shiraishi discloses a semiconductor device that is made by mounting semiconductor elements on both sides of a wiring board having three-dimensional wiring including inner-via holes. According to Shiraishi, a high operating speed and smaller size are made possible by employing a laminated structure of semiconductor elements without using a chip-on-chip configuration. Semiconductor elements are mounted on both sides of a wiring board having three-dimensional wiring including inner via holes so that the semiconductor elements oppose each other via the wiring board. The electrodes of the semiconductor elements are connected with each other by the three-dimensional wiring of the wiring board. [*see* Shiraishi, Abstract]

However, as acknowledged by the Patent Office, Shiraishi does not disclose or suggest the feature of a heat sink having side portions extending towards the planar package surface, the heat sink thermally coupled to the second surface of the semiconductor chip so that heat generated from the at least one semiconductor chip flows towards the heat sink. As Shiraishi does not disclose or suggest a heat sink, it is respectfully submitted that Shiraishi does not disclose or suggest the features of the second surface of the at least one semiconductor chip being adhesively bonded to the heat sink, as recited in independent claims 2, 14 and 23, or the heat sink being substantially thermally isolated from the planar package substrate, as recited in independent claims 3, 15 and 24.

Kato discloses a semiconductor package that includes a semiconductor chip, an interconnection substrate having the semiconductor chip mounted on one surface of the

interconnection substrate, and a package base having the interconnection substrate mounted on one surface of the package base. According to Kato, an optical transmission medium is provided on the package base at a location corresponding to an optical device provided on the interconnection substrate. On the other surface of the package base is provided a receptacle for making an optical connection between an optical fiber cable and the optical transmission medium. Signals are input and/or output via the optical fiber cable connected to the receptacle. [*see* Kato, Abstract]

As disclosed by Kato,

> the package base 80 is provided with a frame 82 and also a lid 83 on the upper face of the package base 80 for protecting the interconnection substrate 20 and the semiconductor chip 10 from the external ambience. The frame 82 and the lid 83 are made of, for example, Kovar alloy. The frame 82 is fixed with *hard-solder* on the upper face of the package base 80 in its peripheral region. The package is sealed with the lid 83 fixed on the frame 82 by *seam welding*. In order to release the heat generated in the semiconductor chip 10, the lid 83 also has contact with the semiconductor chips 10 *via solder with high thermal conductivity*. [Kato, column 7, lines 47-58 (emphasis added)]

Consequently, Kato discloses that frame 82 is *hard-soldered* to the package base 80, the lid 83 is *seam welded* to the frame 82, and the lid 80 is *soldered* to the semiconductor chips 10.

With respect to the rejection of independent claims 2, 14, and 23, in contrast to Kato, exemplary embodiments of the present invention provide for attaching the heat sink to the semiconductor chips with an attachment item, such as an adhesive, that does not thermally isolate the semiconductor chip. For example, a thermally-conductive epoxy can be used as the attachment item. [*see* present application, page 5, paragraph 0015] Therefore, as Kato discloses that the lid 80 is *soldered* to the semiconductor chips 10, it is respectfully submitted that Kato does not disclose or suggest the feature of, for example, the second surface of the at

least one semiconductor chip being *adhesively bonded* to the heat sink. Consequently, it is respectfully submitted that Kato does not address the above-identified deficiencies of Shiraishi noted with respect to independent claims 2, 14 and 23.

With respect to the rejection of independent claims 3, 15 and 24, in contrast to Kato, exemplary embodiments of the present invention provide that the heat sink can be substantially thermally isolated from the planar package substrate. Therefore, as Kato discloses that the frame 82 is *hard-soldered* to the package base 80, it is respectfully submitted that Kato does not disclose or suggest the feature of, for example, the heat sink being *substantially thermally isolated* from the planar package substrate. Consequently, it is respectfully submitted that Kato does not address the above-identified deficiencies of Shiraishi noted with respect to independent claims 3, 15 and 24.

In addition, according to M.P.E.P. § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." [M.P.E.P. § 2143] In other words, "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." [M.P.E.P. § 2143.01] Since neither Shiraishi nor Kato disclose or suggest a combination of features including the features of, for example, the second surface of the at least one semiconductor chip being *adhesively bonded* to the heat sink, or the heat sink being *substantially thermally isolated* from the planar package substrate, it is respectfully submitted

that there is no teaching, suggestion or motivation, either explicitly or implicitly, to combine the references in the manner suggested by the Patent Office. Consequently, it is respectfully submitted that the Patent Office has not established a prima facie case of obviousness. For at least the aforementioned reasons, it is respectfully submitted that the combination of Shiraishi and Kato does not render independent claims 2, 3, 14, 15, 23 and 24 unpatentable.

In addition, according to M.P.E.P. § 2142, "[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art." Furthermore, according to M.P.E.P. § 2143.01, "[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also suggests the desirability of [such modification]." [citing *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)] It is respectfully submitted that there is no disclosure or suggestion in Shiraishi regarding optical interconnection access, any desire for such access or any disclosure or suggestion regarding optics in general. It is respectfully submitted that the Patent Office's stated motivation for combining Kato with Shiraishi "for the purpose of providing means which achieves practical application of optical interconnection technology" is without support in Shiraishi. Therefore, it is respectfully submitted that the Patent Office's attempt to combine Shiraishi and Kato for its rejection based on obviousness is founded upon "knowledge gleaned only from applicant's disclosure." [*see* M.P.E.P. § 2145] Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

Dependent claims 4, 7, 8, 11, 16, 19, 20 25, 27 and 28 variously depend from independent claims 3, 15 and 24, and are, therefore, patentably distinguishable over the

combination of Shiraishi and Kato for at least those reasons stated above with regard to independent claims 3, 15 and 24.

For at least the foregoing reasons, it is respectfully submitted that the combination of Shiraishi and Kato does not render claims 31-33 unpatentable.

For at least the foregoing reasons, it is respectfully submitted that the combination of Shiraishi and Kato does not render the subject matter of claims 2-4, 7, 8, 11, 12, 14-16, 19, 20, 23-25 and 27-33 unpatentable. Accordingly, reconsideration and withdrawal of these grounds of rejection are respectfully requested.

Entry of this Amendment is proper under 37 C.F.R. § 1.116, because the Amendment places the application in condition for allowance for the reasons discussed herein. Furthermore, the Amendment does not raise any new issue requiring further search and/or consideration. For example, claims 2, 3, 14, 15, 23 and 24, which are already under examination, have been amended merely to write these claims in independent form. Dependent claims 4, 7, 8, 11, 12, 16, 19, 20, 25, 27 and 28, also already under examination, have been amended merely to change the dependency of these claims. In addition, the total number of claims in the present Amendment has not changed from the previous Amendment. Entry of the present Amendment is thus respectfully requested.

All of the rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, the Examiner is urged to contact the Applicant's attorney, Andrew J. Bateman, by telephone at (202) 625-3547. All correspondence should continue to be directed to the address given below.

Respectfully submitted,

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